

FIG. 1 PRIOR ATR

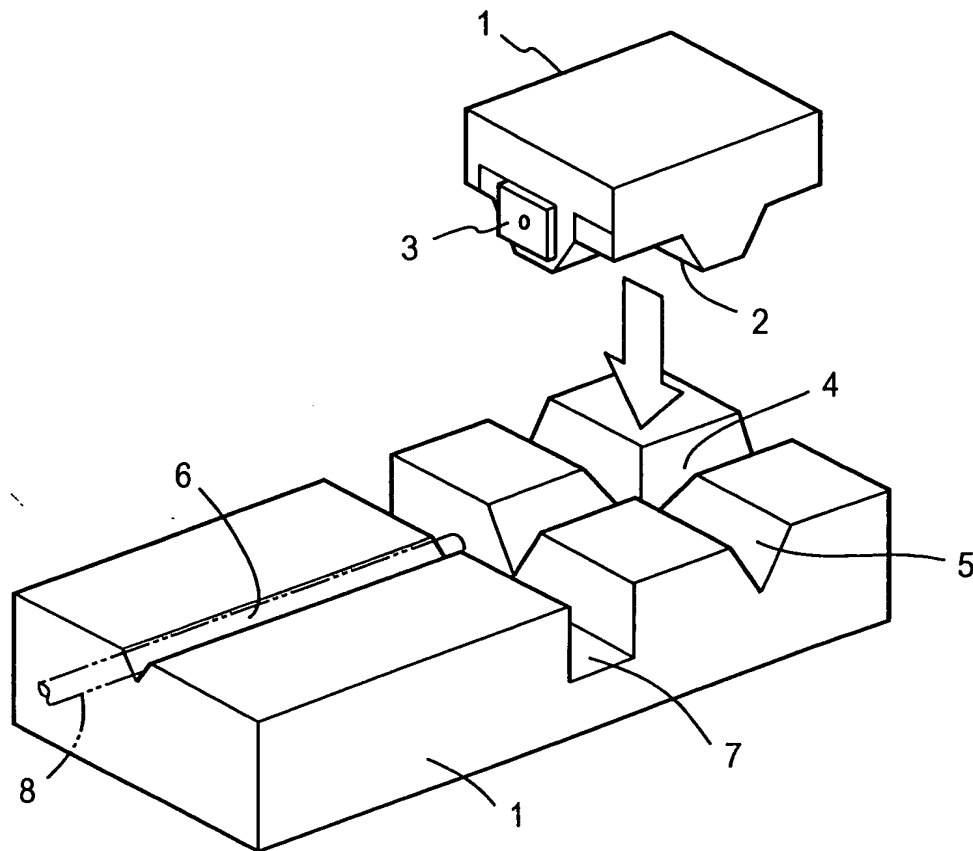


FIG. 2

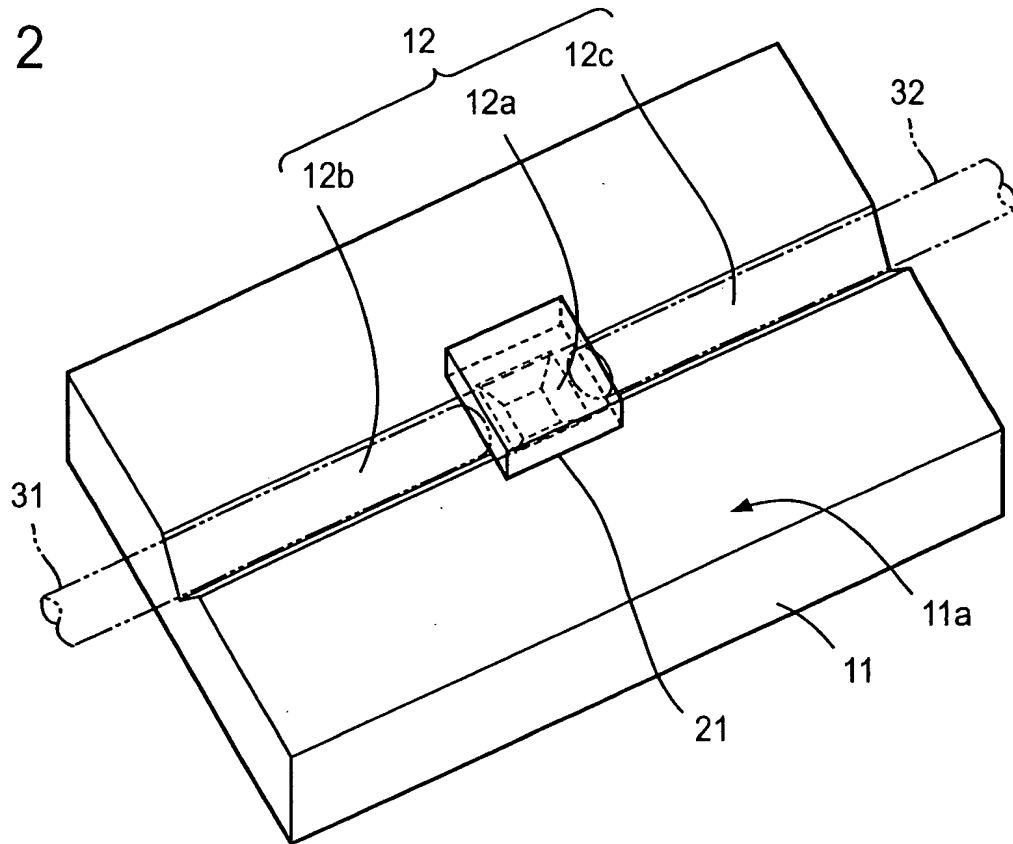


FIG. 3

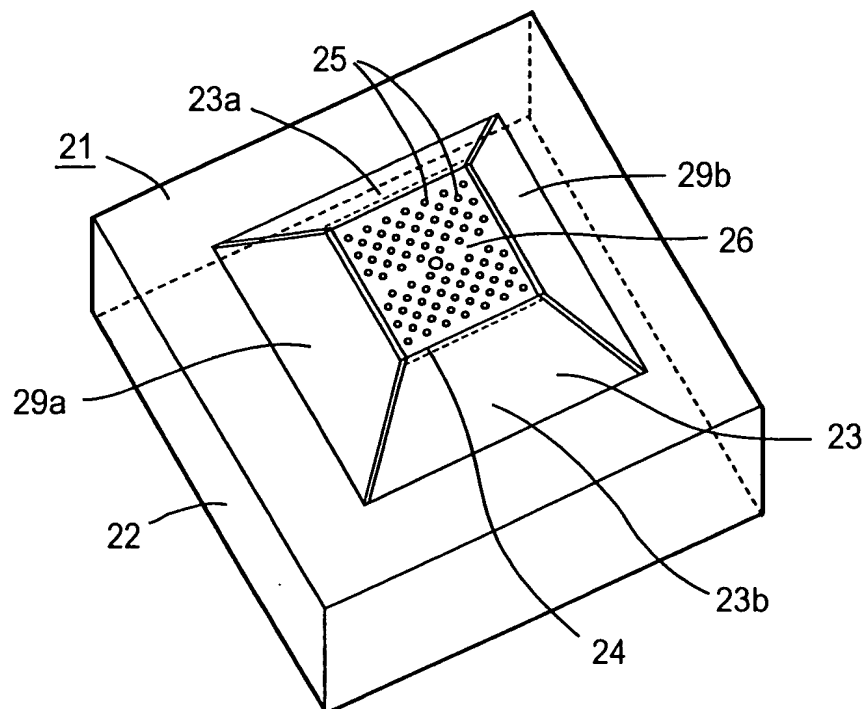




FIG. 6A

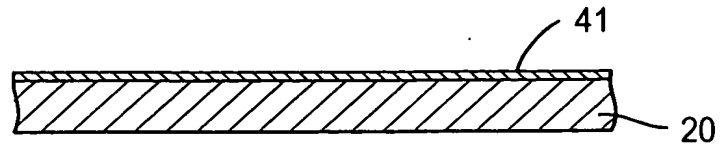


FIG. 6B

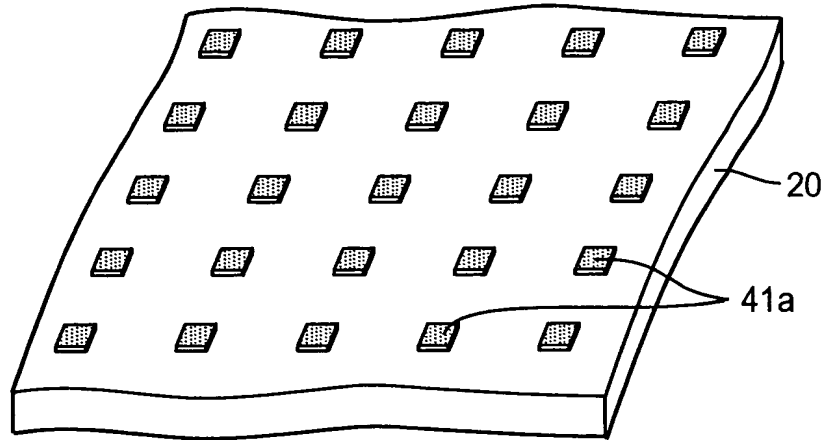


FIG. 6C

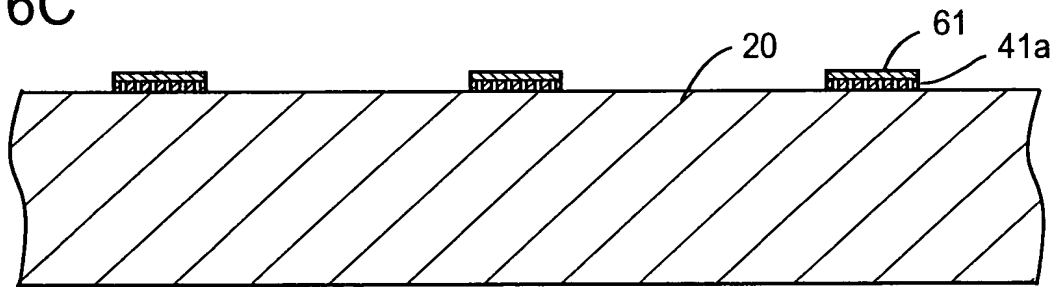


FIG. 6D

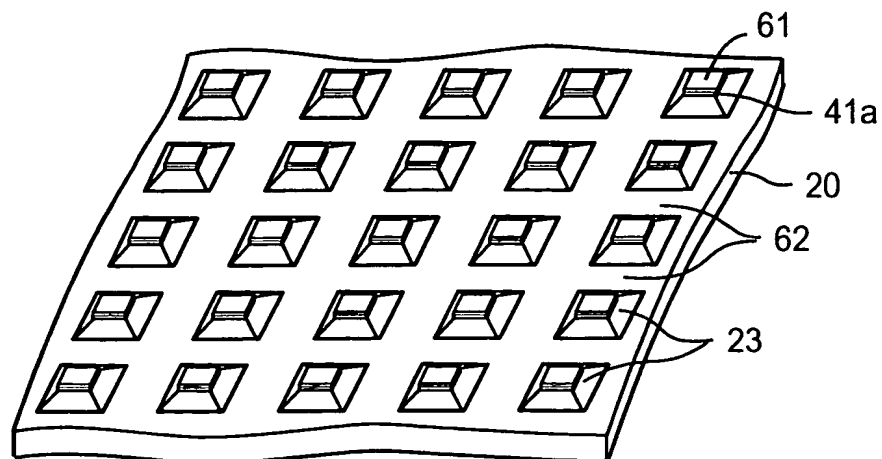


FIG. 6E

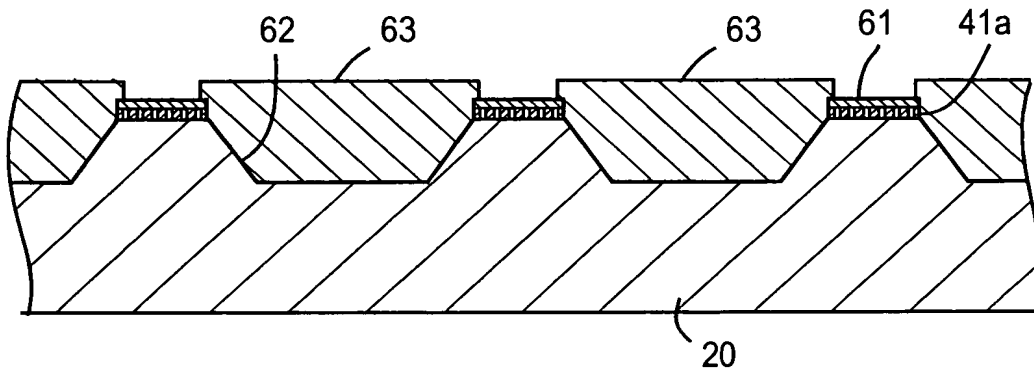


FIG. 6F

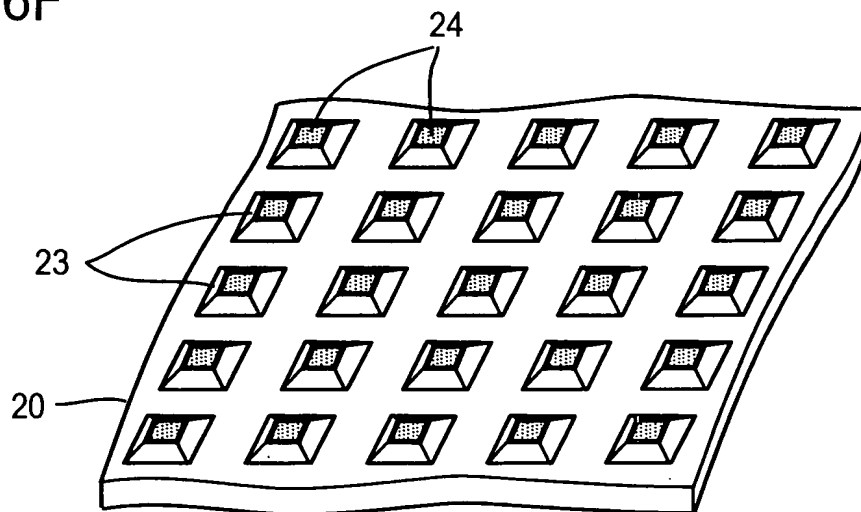


FIG. 6 is a cross-sectional view of a semiconductor device. It shows a central gate stack (21) over a channel region (24). The device includes source/drain regions (31, 32) and a substrate (11). Dimensions D2 and 11a are indicated. Arrows point to features 9 and g.

FIG. 9

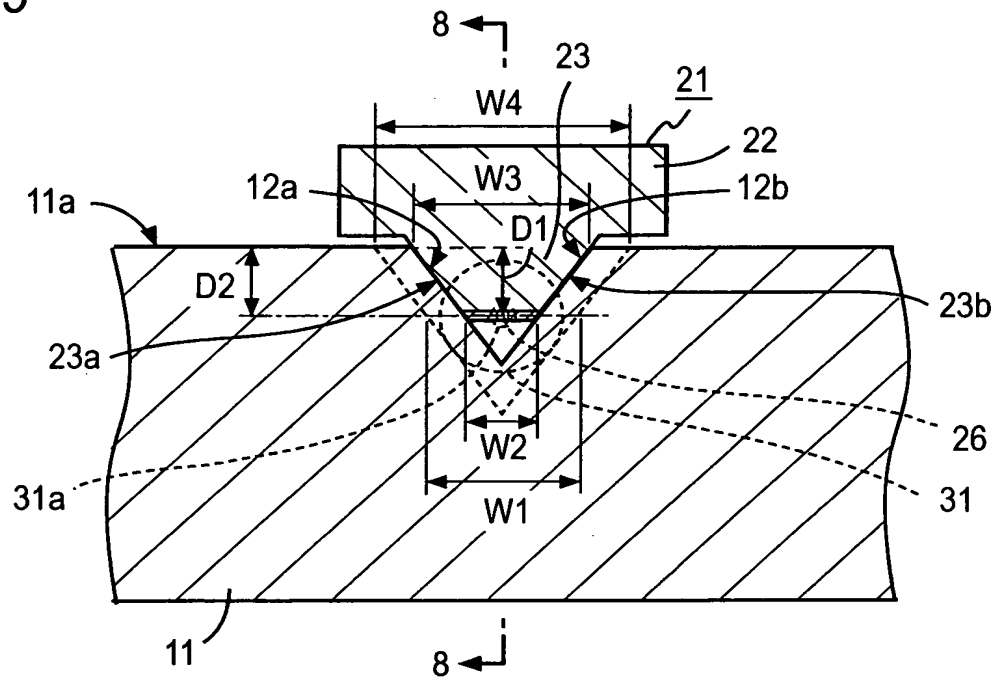


FIG. 10

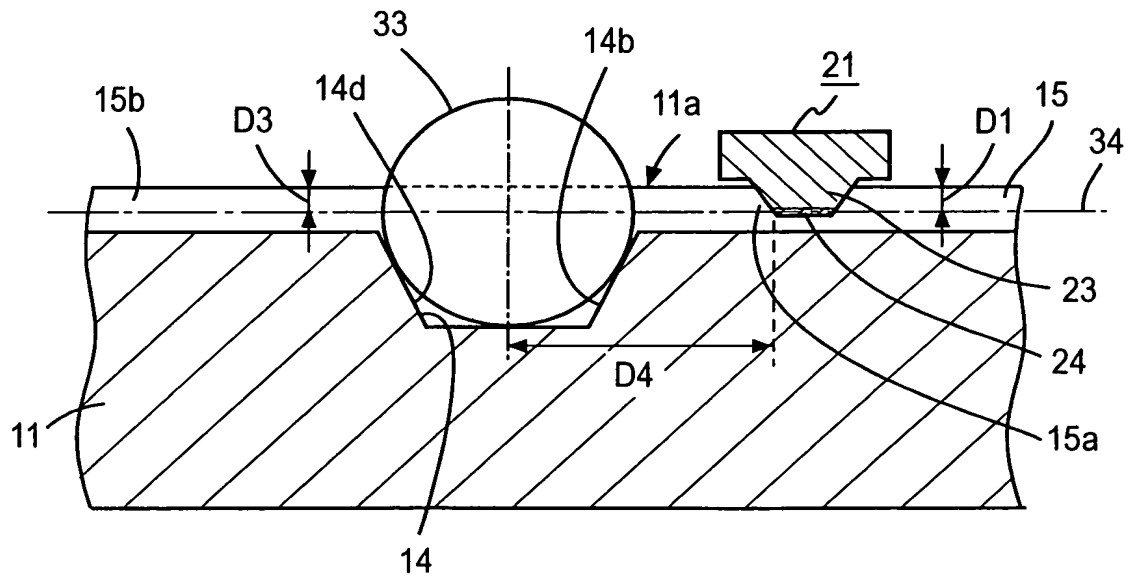


FIG. 11

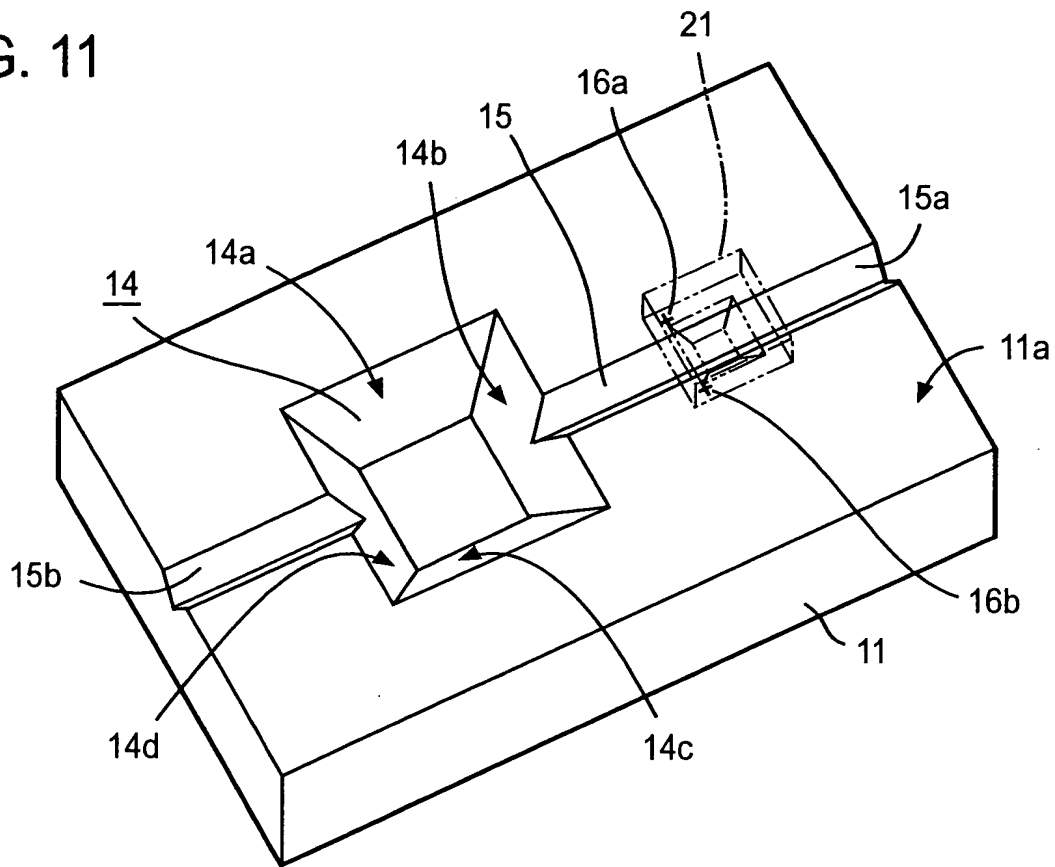


FIG. 12

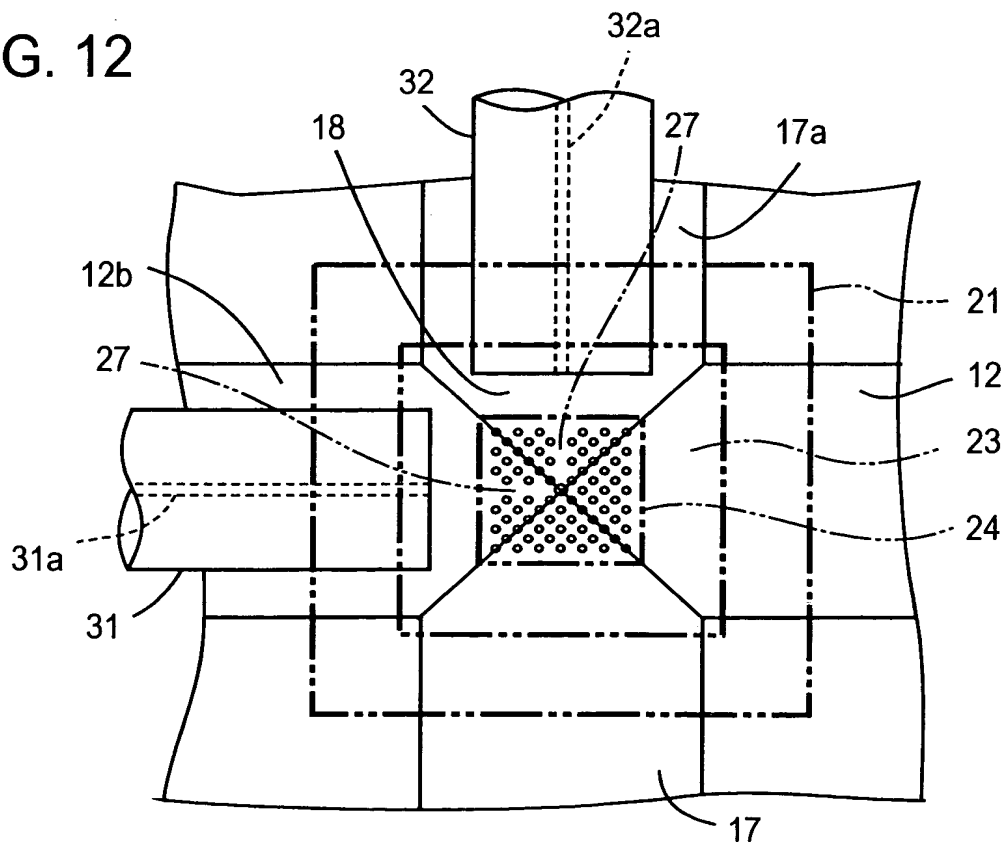




FIG. 13

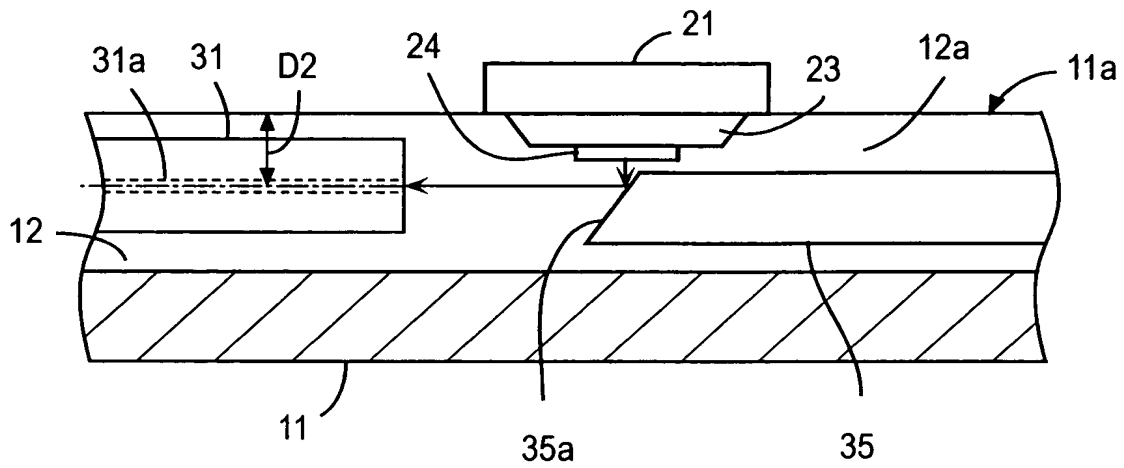


FIG. 14

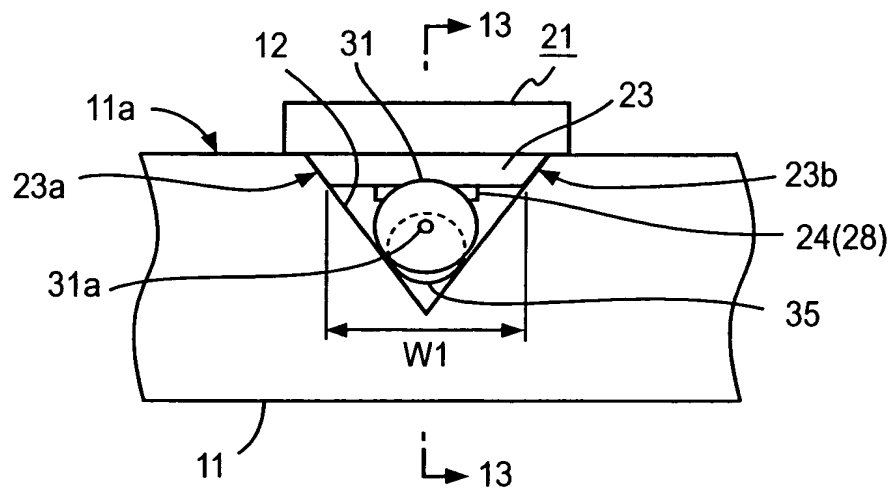




FIG. 17

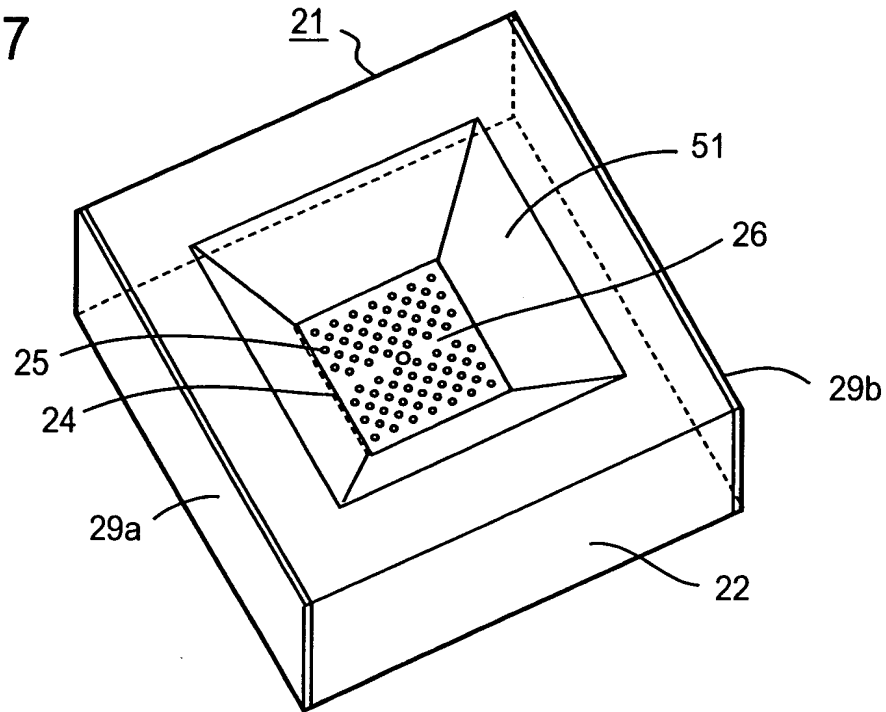


FIG. 18

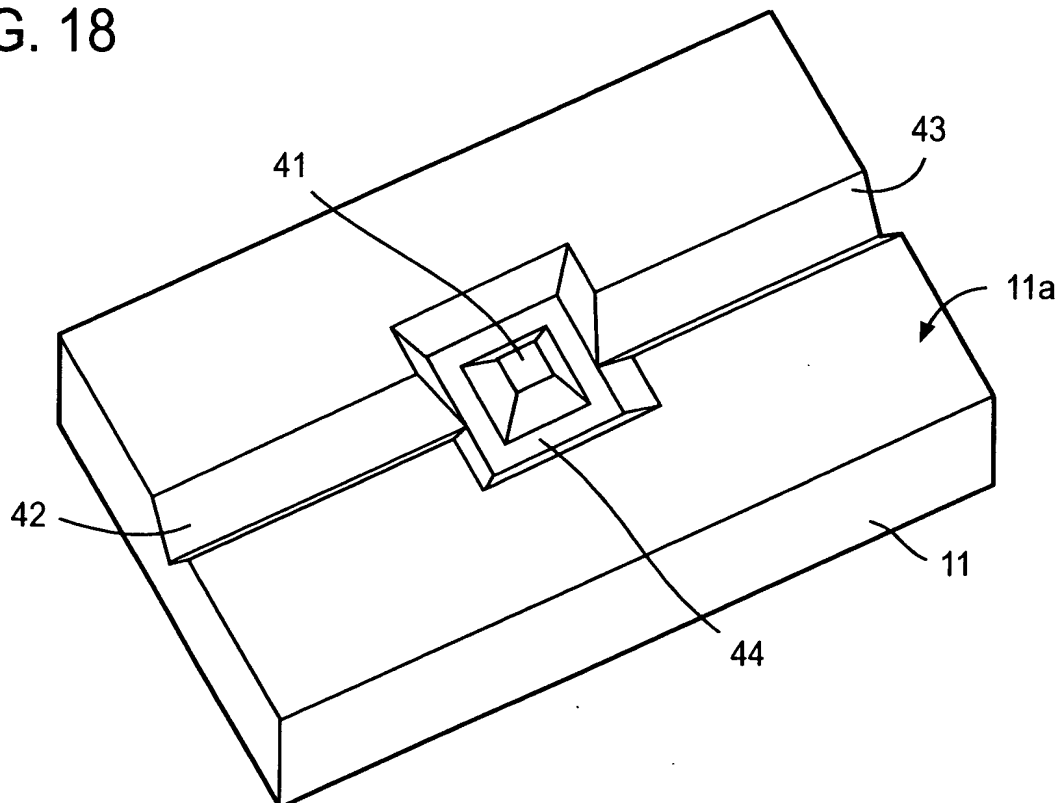
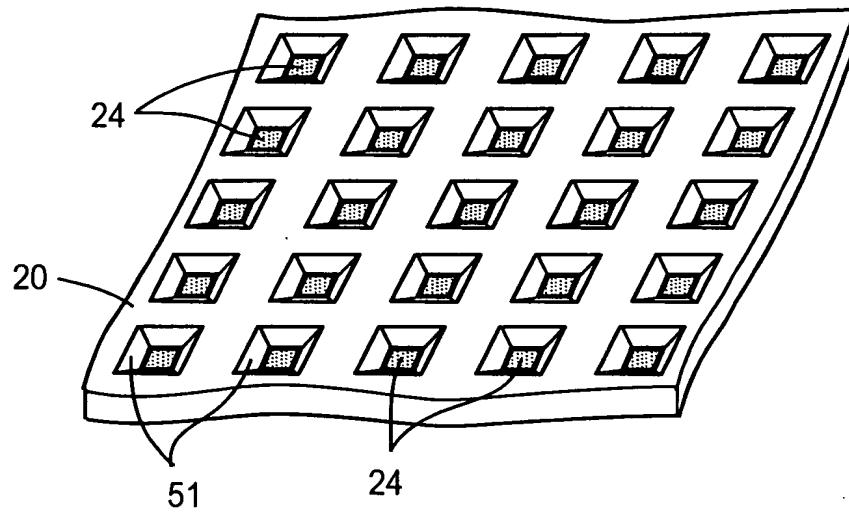


FIG. 19



[illegible]

FIG. 22

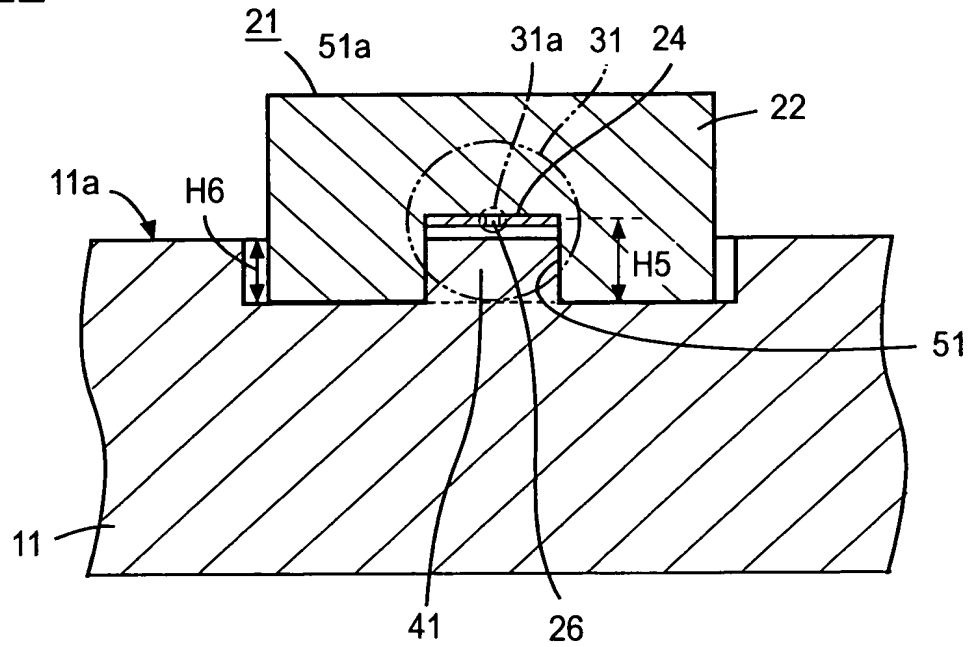


FIG. 23

